WHAT IS CLAIMED IS:

1. A method for improving accuracy of a selection signal provided for a multiplexing circuit, said multiplexing circuit generating an output signal from a plurality of source signals in response to said selection signal, and said method comprising a step of prohibiting said selection signal from toggling when any of said plurality of source signals is at an output-enabled state.
2. The method according to claim 1 wherein said output-enabled state is a high-level state.
3. The method according to claim 1 wherein every adjacent two of said source signals have one-clock difference therebetween, and said plurality of source signals are a series of increasingly lagging signals.
4. The method according to claim 1 wherein every adjacent two of said source signals have one-clock difference therebetween, and said plurality of source signals are a series of increasingly leading signals.
5. The method according to claim 1 wherein said plurality of source signals are generated by a phase-locked loop (PLL) circuit in response to a high frequency signal.
6. A method for generating a selection signal provided for a multiplexing circuit, said multiplexing circuit generating an output signal from a plurality of source signals in response to said selection signal, and said method comprising steps of:

performing an OR operation of said plurality of source signals to obtain an operational output signal; and

latching said operational output signal in an active low manner in response to a selection command to obtain said selection signal.

7. The method according to claim 6 wherein every adjacent two of said source signals have one-clock difference therebetween, and said plurality of source signals are a series of increasingly lagging signals.
8. The method according to claim 6 wherein every adjacent two of said source signals have one-clock difference therebetween, and said plurality of source signals are a series of increasingly leading signals.
9. The method according to claim 6 wherein said plurality of source signals are generated by a phase-locked loop (PLL) circuit in response to a high frequency signal.
10. A device for generating a selection signal provided for a multiplexing circuit, said multiplexing circuit generating an output signal from a plurality of source signals in response to said selection signal, and said device comprising:

an operational circuit receiving and operating said plurality of source signals to obtain an operational output signal; and

a toggle control circuit coupled to said operational circuit and latching said operational output signal under a certain state condition in response to a selection command to obtain said selection signal.

11. The device according to claim 10 wherein said operational circuit is an OR gate.
12. The device according to claim 10 wherein said toggle control circuit is a transparent latch.
13. The device according to claim 10 wherein said certain state condition is an active low condition.